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06ES33

Third Semester B.E. Degree Examination, January 2013

Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Design a minimum two level gate combinational network that detects the presence of six illegal code group (decimal 10 to 15) in a 4 bit that represent BCD code by providing a logic 0 and lighting a red LED. **(08 Marks)**

b. Simplify the following expressions using Karnaugh map. Implement the simplified circuit using the gates as indicated.

i) $f(w, x, y, z) = \sum m(1, 5, 7, 9, 10, 13, 15) + d(8, 11, 14)$ using NAND gates.

ii) $f(A, B, C, D) = \pi m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ using NOR gates. **(12 Marks)**

2 a. Simplify using Quine McCluskey minimization technique

$Y(A, B, C, D) = \sum m(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$ **(12 Marks)**

b. Simplify the following Boolean function using variable entered map technique of taking z as the map entered variable:

$f(w, x, y, z) = \sum m(3, 5, 6, 7, 8, 9, 10) + dc(4, 11, 12, 14, 15)$ **(08 Marks)**

3 a. Design a 4 to 16 decoder using 2 to 4 decoders with active low enable and active low outputs. **(08 Marks)**

b. Design a keypad interface to a digital system using ten line to four line encoder. **(06 Marks)**

c. Design a binary full subtractor using basic gates. **(06 Marks)**

4 a. Implement the expression $s = ad + b\bar{c} + bd$ using 4:1 mux. Choose b and d as select lines. **(10 Marks)**

b. Design a combinational circuit that accepts two unsigned 2-bit binary number and provides 3 outputs.

Input : word $A = A_1A_0$ word $B = B_1B_0$

Output : $A = B$, $A > B$, $A < B$. **(10 Marks)**

PART – B

5 a. Explain the working of Master-Slave JK flip-flop with functional table and timing diagram. Show how race around condition is overcome. **(08 Marks)**

b. Explain switch debouncing and its elimination using SR latch. **(06 Marks)**

c. Obtain characteristic equations of JK and SR flip-flops. **(06 Marks)**

6 a. Explain the operation of Ring counter and twisted ring counter using shift register with the help of diagram. **(08 Marks)**

b. Design a synchronous mod 6 counter using clocked JK flip-flop. (sequence 0, 2, 3, 6, 5, 1, 0) **(12 Marks)**

7 a. With block diagram, write the two distinct models used in designing synchronous sequential logic circuit. **(06 Marks)**

b. Give output function, excitation table, transition table, state table and state diagram by analyzing the sequential circuit shown in Fig.Q7(b). **(14 Marks)**

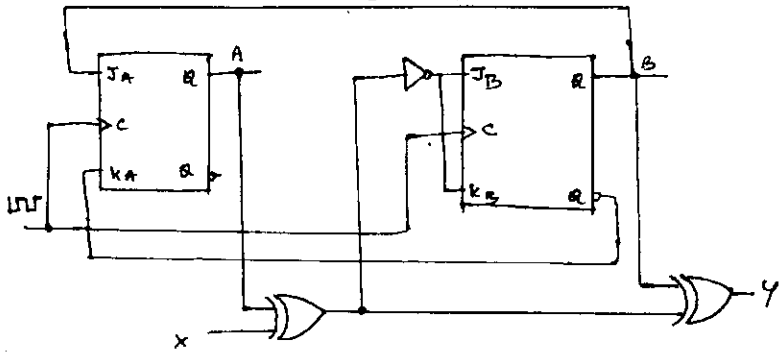

Fig.Q7(b)

8 a. Construct a mealy state diagram that will detect a serial sequence of 10110 when the input poltroon has been detected cause an output z to be asserted high. **(08 Marks)**

b. Design a clocked sequential circuit that operates according to the state diagram shown IN Fig.Q8(b). Implement the circuit using T flip-flop. **(12 Marks)**

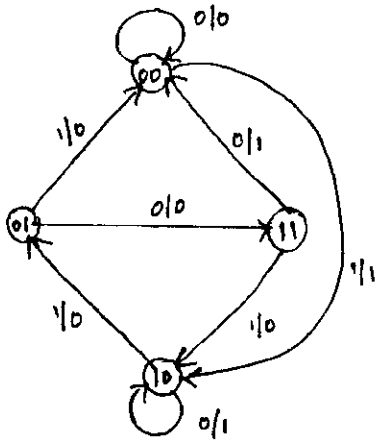

Fig.Q8(b)

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